

What is claimed is:

1           1. A memory cache bank prediction unit for use in a processor having a plurality of  
2 memory cache banks, comprising:  
3           an input port configured to receive an instruction; and  
4           an evaluation unit coupled to said input port and configured to predict which of the  
5 plurality of memory cache banks is associated with the instruction.

1           2. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is  
2 configured to predict which of the plurality of memory cache banks is associated with the  
3 instruction based on information related to at least one of: (I) a bank history; (ii) a control flow;  
4 and (iii) a load target-address information.

1           3. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is  
2 configured to perform a plurality of binary evaluations and predict which of the plurality of  
3 memory cache banks is associated with the instruction based on a majority vote of the plurality  
4 of binary evaluations.

1           4. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is  
2 configured to perform a plurality of evaluations, each evaluation being associated with a  
3 confidence, and predict which of the plurality of memory cache banks is associated with the  
4 instruction based on the plurality of evaluation confidences.

1           5. The memory cache bank prediction unit of claim 4, wherein said evaluation unit is  
2 configured to predict which of the plurality of memory cache banks is associated with the  
3 instruction based on obtaining a sum of evaluation confidences above a threshold value.

1           6. A method of scheduling an instruction to a processor having a plurality of memory  
2 cache banks, comprising:  
3           predicting which of the plurality of memory cache banks is associated with the  
4 instruction; and  
5           scheduling the instruction for execution based on the predicted memory cache bank.

1           7. The method of claim 6, wherein said predicting is based on information related to at  
2 least one of: (i) a bank history; (ii) a control flow; and (iii) a load target-address information.

1           8. The method of claim 6, wherein said predicting comprises performing a plurality of  
2 binary evaluations and the prediction is based on a majority vote of the plurality of binary  
3 evaluations.

1           9. The method of claim 6, wherein said predicting comprises a plurality of evaluations,  
2 each evaluation being associated with a confidence, and the prediction is based on the plurality of  
3 evaluation confidences.

1           10. The method of claim 9, wherein said predicting is based on a sum of evaluation  
2           confidences above a threshold value.

1           11. An article of manufacture comprising a computer-readable medium having stored  
2           thereon instructions adapted to be executed by a processor having a plurality of memory cache  
3           banks, the instructions which, when executed, cause the processor to schedule an instruction,  
4           comprising:

5           predicting which of the plurality of memory cache banks is associated with the  
6           instruction; and

7           scheduling the instruction for execution based on the predicted memory cache bank.

1           12. A processor having a first memory cache bank and a second memory cache bank,  
2           comprising:

3           a memory cache bank prediction unit configured to predict which of the plurality of  
4           memory cache banks is associated with an instruction; and

5           a scheduler coupled to said memory cache bank prediction unit and configured to  
6           schedule the instruction for execution based on the predicted memory cache bank.

1           13. A processor having a first memory cache bank and a second memory cache bank,  
2           comprising:

3           a memory cache bank prediction unit;

4           a scheduler coupled to said memory cache bank prediction unit;

5 a first instruction pipeline between said scheduler and the first memory cache bank; and  
6 a second instruction pipeline between said scheduler and the second memory cache bank;  
7 wherein an instruction is placed in both said first instruction pipeline and said instruction  
8 pipeline.

1 14. The processor of claim 13, wherein instructions in the first pipeline are unable to  
2 access information in the second memory cache bank and instruction in the second pipeline are  
3 unable to access information the first memory cache bank.

1 15. The processor of claim 14, wherein an instruction in the first instruction pipeline is  
2 discarded if it needs to access information in the second memory cache bank.  
3

4 16. The processor of claim 13, wherein said prediction unit predicts based on information  
5 related to at least one of: (I) a bank history; (ii) a control flow; and (iii) a load target-address  
6 information.  
7

1 17. The processor of claim 13, wherein said prediction unit performs a plurality of binary  
2 evaluations and the prediction is based on a majority vote of the plurality of binary evaluations.

1 18. The processor of claim 13, wherein said prediction unit performs a plurality of  
2 evaluations, each evaluation being associated with a confidence, and the prediction is based on  
3 the plurality of evaluation confidences.

1           19. The processor of claim 18, wherein said prediction unit predicts based on a sum of  
evaluation confidences above a threshold value.

1           20. A method of executing an instruction in a processor having (I) a first instruction  
2 pipeline between a scheduler and a first memory cache bank and (ii) a second instruction pipeline  
3 between the scheduler and a second memory cache bank, comprising:  
4           predicting which of the memory cache banks is associated with the instruction; and  
5           processing the instruction in both the first instruction pipeline and the second instruction  
6 pipeline.

1           21. An article of manufacture comprising a computer-readable medium having stored  
2 thereon instructions adapted to be executed by a processor having (I) a first instruction pipeline  
3 between a scheduler and a first memory cache bank and (ii) a second instruction pipeline  
4 between the scheduler and a second memory cache bank, the instructions which, when executed,  
5 cause the processor to execute an instruction, comprising:  
6           processing the instruction in both the first instruction pipeline and the second instruction  
7 pipeline.